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A hybrid model for computationally efficient fatigue fracture simulations at microelectronic assembly interfaces

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Abstract

Modern microelectronic assemblies are heterogeneous, layered structures joined by interconnects made of solder alloys with low homologous temperatures. The solder interconnections join devices to circuit boards and they fail by thermal fatigue fracture at their interfaces either to the device or to the circuit board. Predicting the fatigue fracture of the solder interconnections is a challenge due to the fact that they undergo large inelastic deformations during temperature cycling tests. In this paper we develop a hybrid approach inspired by cohesive zone fracture mechanics and the Disturbed State Concept to predict the crack trajectory and fatigue life of a solder interconnection subjected to both isothermal temperature cycling and anisothermal temperature cycling conditions (representing the two common accelerated test conditions for microelectronic products). A hybrid computational approach is used in which a first order approximation of the disturbance is used to estimate incremental cycles to criticality and thereby propagate the crack. The modeled crack fronts and the fatigue lives are validated through a comparison to results from the two types of accelerated tests. Overall, the model is shown to predict the fatigue life of the critical interconnection in the assembly to within 20% of the experimentally determined life. More importantly, the predicted crack trajectory is demonstrated to agree very well with the experimentally observed trajectory. Strikingly, the microscopically observed microstructural changes during crack propagation from that corresponding to creep fatigue to that of shear overload were found to be excellently correlated with the rate of change of the disturbance calculated in the model.

Keywords: Cohesive zone models; Disturbed state concept; Solder interconnections; Thermal fatigue fracture

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1. Introduction

Cyclic loading is very common in many engineering systems such as microelectronics, automobiles and aircrafts. The systems include those exposed to pure mechanical cyclic loadings, temperature cyclic loadings, or both. In general, the experimental testing accompanied by numerical modeling of fatigue crack growth remains a relatively less explored research topic. This is also true for fatigue crack growth along the interfaces of microelectronic assemblies.

Microelectronic components are assembled to circuit boards using solder interconnections (see Fig. 1); eutectic Sn–37 wt%Pb alloy is a common material for the solder interconnections. The fatigue lives of these interconnections are determined by the combined effects of component design, assembly process, and use environment. However, to qualify a product design or to screen defective parts, accelerated temperature cycling tests are carried out or simulated. A common accelerated test is to subject the assembly to a uniform temperature rise of 100 °C from 0 °C. An alternative, and relatively new, test is to generate anisothermal conditions (similar to those that are generated when the devices are powered) through localized heating of the components, but ensuring a temperature range of 100 °C at the solder interconnections.

Empirical models are most commonly used to estimate the fatigue life of solder interconnections under the accelerated test conditions (see Lee et al., 2000, for instance). They are often related to the stress–strain behavior at a point in the interconnection over one cycle and include a measurable physical quantity such as inelastic strain range, $\Delta\varepsilon_p$, or the inelastic dissipation in one cycle, ΔW. A difficulty with the empirical life prediction schemes is that effects of geometry, material behavior, and loading complexity are confounded and the underlying physical mechanisms causing the fracture are usually unknown or cannot be defined. To capture the physics of failure accurately, non-empirical models that describe progressive material degradation and their physical manifestation through the growth of a fatigue crack are necessary.

The commonly used fatigue crack growth models such as the Paris equation (Paris and Erdogan, 1963) assume small scale yielding, constant amplitude loading and self-similar crack growth conditions. In general, for fatigue crack growth along interface, the driving processes at the crack tip cannot be assumed to be independent of geometry and mode mixity. Commonly, the extension of Paris law to systems undergoing plastic yielding is made using the ΔJ-integral (Dowling and Begley, 1976). In the context of solder interconnections which undergo large scale yielding and significant crack growth (see Fig. 1), the assumptions of small cracks, small strains, and deformation theory of plasticity inherent in ΔJ-integral (Anderson, 1995) may not be applicable. In general, the predictive ability of Paris' law is dependent on the satisfaction of the conditions inherent in its formulation, and the common use of ad hoc modifications to account for

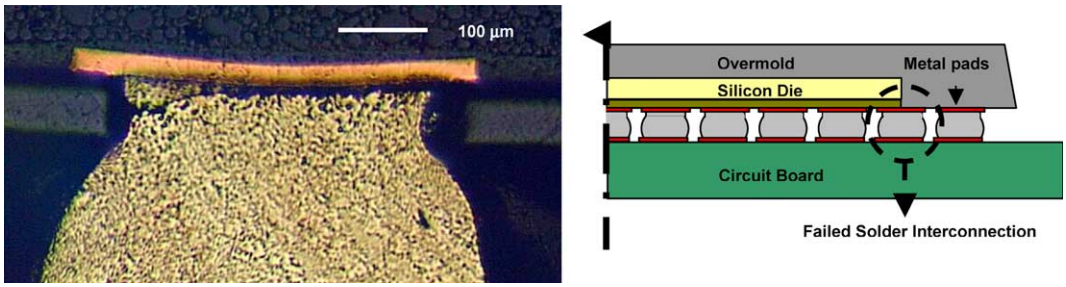

Fig. 1. A typical crack through solder joint interface in an electronic assembly. The solder alloys typically undergo significant plastic and creep deformation during temperature cycling and the cracks run through the entire length of the interface. The circle in dashed lines indicates the location of the critical solder interconnection.

non-ideal conditions has been suggested as indicative of an inability to capture the essential physics of fatigue crack growth (Nguyen et al., 2001).

An alternative approach to classical fracture mechanics is to model fatigue crack growth through a cohesive zone law. The idea of a cohesive zone was first introduced by Barrenblatt (1962) and Dugdale (1960). Within the cohesive framework, the material behavior is divided into two parts: one that uses continuum theory with no damage to relate stress and deformation in the bulk material, and the second that uses cohesive zone to describe the integrity of the interface near the crack tip. The cohesive zone models are based on a prescribed relationship between traction and corresponding crack opening displacement, which is specific for each material and is independent of the geometry or global loading conditions. Cohesive law of fracture provides the ability to address the problems that are difficult to address under constraints of classical fracture mechanics such as crack initiation, large-scale yielding condition, or irreversible unloading (Hutchinson and Evans, 2000). The shape of surface traction-opening displacement relationship takes many forms. However all cohesive laws share commonality in that they contain at least two material parameters to define the shape of traction-opening displacement relation (typically maximum cohesive traction and characteristic opening displacement).

Cohesive zone models in which the loading curve is not retraced during unloading (irreversible cohesive law, Needleman, 1992; Camacho and Ortiz, 1996) are essential in modeling fatigue crack growth. Recently fatigue crack growth using the irreversible cohesive zone models have been demonstrated in the literature (de-Andrés et al., 1999; Nguyen et al., 2001; Roe and Siegmund, 2003).

In general, a challenge to using cohesive zone models is the availability of the cohesive laws for materials of interest. At the present time, cohesive laws do not appear to have been developed for solder alloys in general and for the most commonly used eutectic Sn–37 wt%Pb solder alloy in particular. However, since the Crack Tip Opening Displacement (CTOD) in ductile materials is a function of the crack tip plasticity (Anderson, 1995), intuitively, one expects that a two-parameter criterion based on crack-tip plasticity would potentially capture the crack growth behavior that a cohesive law would predict. Thus, in the present paper, we develop and apply a two-parameter disturbance measure based on crack-tip equivalent plastic strain to predict fatigue crack growth at the interface of solder interconnections. In the following section, we develop the disturbance measure and illustrate the similarity of its mathematical form to the irreversible cohesive zone model of de-Andrés et al. (1999). We then describe the procedure for evaluating and incrementing the disturbance within a finite element code. Following this, we apply the procedure to simulate fatigue crack growth in a microelectronic package under both isothermal and anisothermal test conditions. Finally, we compare the results of the simulation to experimentally determined crack fronts and fatigue lives.

2. A hybrid model for fatigue fracture simulation

We begin by using the irreversible cohesive law of de-Andrés et al. (1999) (illustrated in Fig. 2) to motivate the disturbance measure used in the present study. We briefly repeat the salient aspects of the cohesive model used by de-Andrés et al. (1999) before describing the approach used in the present study. de-Andrés et al. (1999) used a Smith–Ferrante traction–separation relation of the form

$$t(\delta) = e\sigma_c \frac{\delta}{\delta_c} \exp\left[-\frac{\delta}{\delta_c}\right], \quad \text{if } \delta = \delta_{max} \quad \text{and} \quad \dot{\delta} \geqslant 0 \tag{1}$$

where σ_c is the maximum cohesive traction (also denoted as cohesive strength) and δ_c is the characteristic opening displacement. The quantity σ_c describes the maximum cohesive normal traction. During unloading (when the local cohesive surface does not undergo loading), two mechanisms can be used depending upon the material behavior: ductile and brittle unloading. These mechanisms are both defined as the straight line starting from the point on the loading envelop (δ_{max}), where the global (or local) system begins unloading.

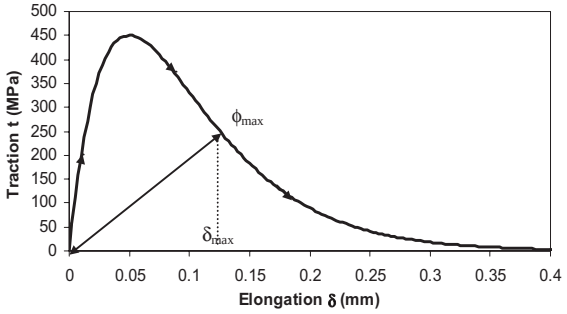

Fig. 2. Irreversible cohesive law showing a Smith–Ferrante loading and unloading to the origin (de-Andrés et al., 1999).

The unloading path can be parallel to the initial tangent stiffness in the case of ductile unloading (due to inelasticity causing residual separation) and may go directly to the origin in the case brittle unloading.

The potential from which the traction corresponding to Eq. (1) is derived is

$$\phi(\delta) = e\sigma_c\delta_c\left[1 - \left(1 + \frac{\delta}{\delta_c}\right)e^{-\delta/\delta_c}\right] \tag{2}$$

The total area underneath the curve of Eq. (1) defines the critical energy release rate, G_c, from a standard application of the J-integral.

$$G_c = \int_0^\infty t\,d\delta = e\sigma_c\delta_c \equiv \phi_\infty \tag{3}$$

de-Andrés et al. (1999) defined a damage parameter, D as:

$$D = \frac{\phi(\delta_{max})}{G_c} \tag{4}$$

Therefore, at any δ_{max},

$$D = 1 - \left(1 + \frac{\delta_{max}}{\delta_c}\right)\exp\left[-\frac{\delta_{max}}{\delta_c}\right] \tag{5}$$

Upon cyclic loading and unloading the damage value increases with the number of cycles (causing an increase in δ_{max}) and eventually the damage is sufficient to form a new surface when the cohesive surface loses its integrity.

Desai and Toth (1996), Desai et al. (1997), Desai and Whitenack (2001), and Desai (2002) proposed a scalar, isotropic disturbance measure as part of a unified constitutive behavior for solder alloys that allowed for the inclusion of elastic, plastic and creep strains, microcracking, degradation and fatigue failure. A general form of the disturbance function proposed by Desai is:

$$D = D[\xi, w, S, \phi, t(N), T, \alpha_i] \tag{6}$$

where ξ denotes an internal variable such as the plastic strain trajectory, w is the dissipated energy, S is entropy, ϕ is free energy, t is time or number of loading cycles N, T is the temperature and α_i denotes factors such as environmental effects. The disturbance function may be simplified to:

$$D = D[\xi(t, T, \alpha_i)]$$

where ξ is affected by time, temperature and α_i. Assuming further that the microstructural changes are attributed to deviatoric plastic strain trajectory ξ_D, and defining the disturbance function using Weibull functions (Weibull, 1951), we may express the disturbance as:

$$D = 1 - \left[1 + \left(\frac{\xi_D}{\xi_c}\right)^{\beta}\right]^{-\gamma} \tag{7}$$

where ξ_c, β, and γ are material constants. The above equation may be further simplified and re-stated in the following form:

$$D = 1 - \exp\left[-\left(\frac{\xi_D}{\xi_c}\right)^{z}\right] \tag{8}$$

where ξ_D is the equivalent inelastic strain calculated from the instantaneous plastic strain and the time-dependent creep strain; ξ_c and z are material constants. In the present study, we propose the use of the disturbance in Eq. (8) as indicative of the local accumulation of damage and its critical value at the crack tip as indicative of the condition under which a crack would propagate.

Clearly, the mathematical forms of the damage relations in Eqs. (5) and (8) are similar for ductile materials. The accumulated damage and disturbance in both relations is exponential, but the rate of damage accumulation is more rapid in Eq. (8) since the value of z is typically less than 1 (Fig. 3 is for a z value of 0.676, which is the average value over the temperature range of −50 °C to +150 °C, corresponding to a near-eutectic Sn–40 wt%Pb solder alloy). Furthermore, in Eq. (5), the driver for fracture is the incremental opening of the crack after unloading and reloading (see Fig. 2) resulting in an increased δ_{max}. Thus, one may postulate a direct (albeit difficult to quantify) relation between the increase in the equivalent plastic strain and the extension δ_{max} in the cohesive zone.

The parameters ξ_c and z in Eq. (8) were determined by Desai et al. (1997) from the relation between load drop and inelastic strain during fatigue tests conducted by Solomon (1985). Solomon's fatigue tests were carried out on cast Sn–40 wt%Pb solder specimen. In the current study the behavior of the eutectic Sn–37 wt%Pb is assumed to be nearly the same as that of the Sn–40 wt%Pb alloy. Thus, for eutectic Sn/Pb solder, the average value of the parameters over the temperature range of −50 °C to +150 °C were determined as $\xi_c = 29.26$, $z = 0.676$. Furthermore, the critical value at which the material changes from relatively intact state to fully adjusted state was chosen as $D_c = 0.85$, however as is shown later, the accuracy of the simulations are not critically dependent on this value.

A drawback of the cumulative damage accumulation models is the computational cost associated with modeling every loading cycle. Empirical strategies based on experimentally observed load drop during fatigue test have been proposed by Desai and Whitenack (2001) to alleviate computational expense. Here, to

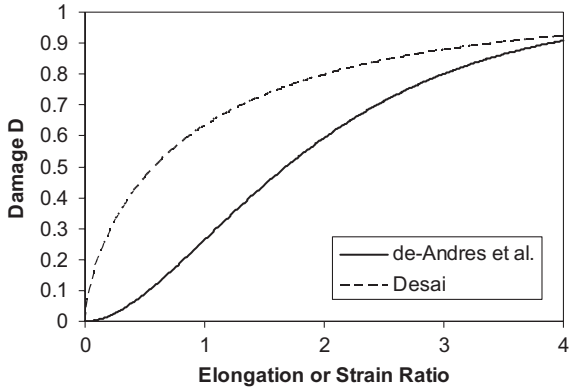

Fig. 3. Damage and disturbance accumulation as a function of elongation ratio or strain ratio (fractions of characteristic values).

achieve computational efficiency, the disturbance state is extrapolated to advance the crack using a one-term Taylor expansion similar to de-Andrés et al. (1999):

$$D_{n+1} \approx D_n + \left.\frac{\partial D}{\partial N}\right|_n (N_{n+1} - N_n) \tag{9}$$

Here, N_{n+1} and N_n are the number of cycles of fatigue life at the end of $n+1$ and n iterations, respectively. D_{n+1} and D_n are the values of the disturbance parameter associated with N_{n+1} and N_n cycles. The rate of disturbance change over a cycle $(\partial D/\partial N)_n$ is calculated using finite difference derivatives. The number of cycles for crack advance is calculated by advancing the disturbance to critical state, that is, by determining the number of cycles when D_{n+1} equals to D_c.

3. Finite element analysis of accelerated cycling tests

As part of an earlier study (Towashiraporn et al., 2004a,b), a Chip-Scale Package (Fig. 4), in which the solder joints are damaged predominantly in shear, was tested under anisothermal power cycling (simulates the powering of the device and hence the terminology) and isothermal temperature cycling conditions. In the former, a local Peltier heater was used external to the device to heat the component resulting in anisothermal conditions in the assembly at every instant. In the latter, a uniform temperature was imposed on the assembly at every instant. The details of the tests, post-failure microscopic analysis as well as elementary *empirical* life modeling of the tested packages are described in Towashiraporn et al. (2004a,b). In the tests, a cyclic temperature excursion between the extremes of 0 °C and 100 °C was maintained at the solder interconnections. This was done in the case of power cycling by a temperature controller driven using the temperature sensed by a thermocouple embedded in the solder interconnection array. The dwell period in the isothermal cycling test was 10 min. During power cycling, approximately 2.5 min of dwell period was felt to

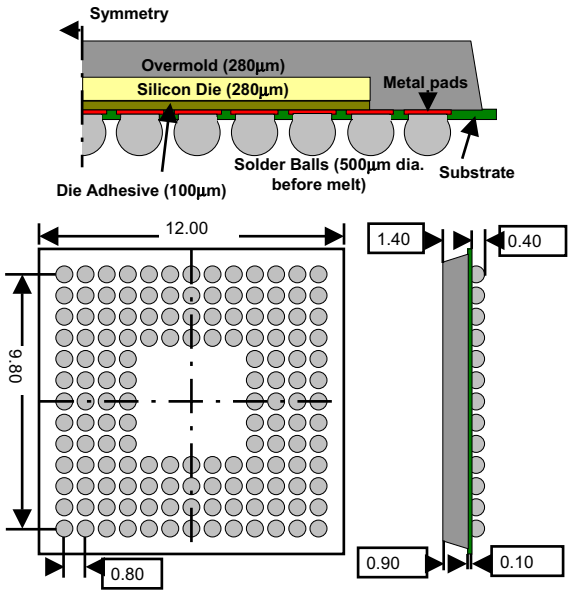

Fig. 4. Schematic diagram of test vehicle TI 144 GGU containing 144 solder interconnections. The dimensions are in mm unless stated explicitly. The dimensions in the top figure refer to thickness.

be sufficient for significant relaxation of solder stress to occur when compared to the 10-min dwell period used in temperature cycling. This is consistent with the findings of Shiratori and Yu (1997).

In the present study, we used the refined finite element models of Towashiraporn et al. (2004b) to analyze fracture propagation and life prediction using the earlier described hybrid model. Since the power cycling test condition involves complex, transient, anisothermal condition, transient heat transfer analysis using temperature-dependent convective heat transfer coefficients was carried out. The resulting nodal temperature solutions were then exported in temporal and spatial domains to the subsequent elastic–plastic–creep analysis. The details of the empirical life modeling including an extensive study of sources and effects of error in finite element analysis and the values of material properties are described by Towashiraporn et al. (2004b).

The finite element model used (Fig. 5) contained 23,480 linear brick and wedge elements. Only one-eighth of the package was modeled due to symmetry. Symmetry boundary conditions were applied on symmetry planes (no displacement normal to the planes). The central node at the bottom of the package was constrained in all directions to prevent any rigid body motion. The critical solder interconnection was earlier determined through post-failure microscopic analysis (Fig. 6) conducted using both optical and scanning electron microscopes. The critical interconnection was meshed with hexahedral elements. Care was taken to ensure good aspect ratio, especially along the bonded interface between the solder interconnection and the metal pad.

In the first set of models, to reduce computational effort, a two-staged "global-local" finite element modeling procedure was executed in which a global, coarser model was used to extract boundary conditions for a local refined substructure of the critical solder interconnection. The displacements on the boundary of the

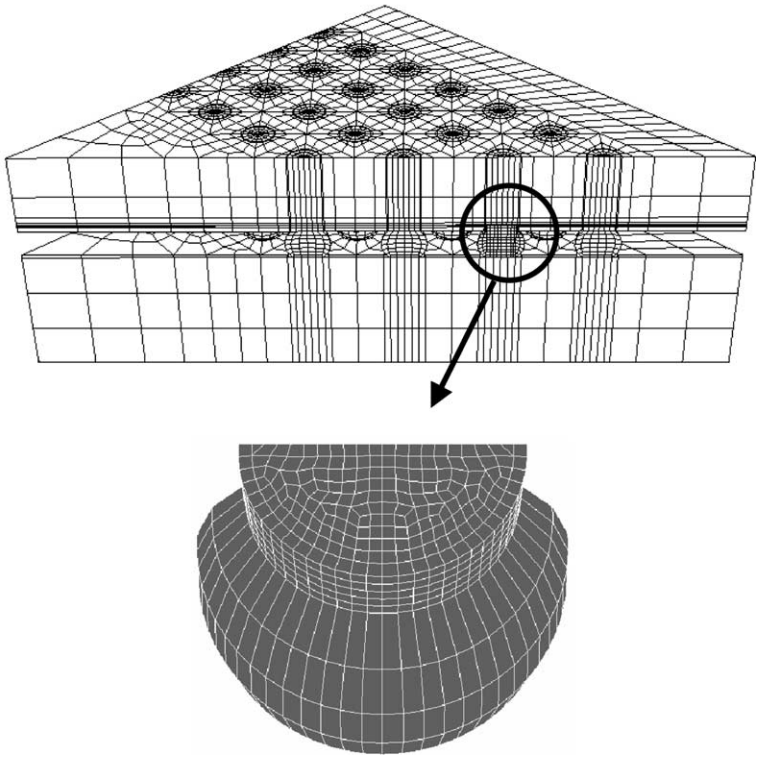

Fig. 5. Finite element model of the component assembly and the refined model used for the critical solder interconnection.

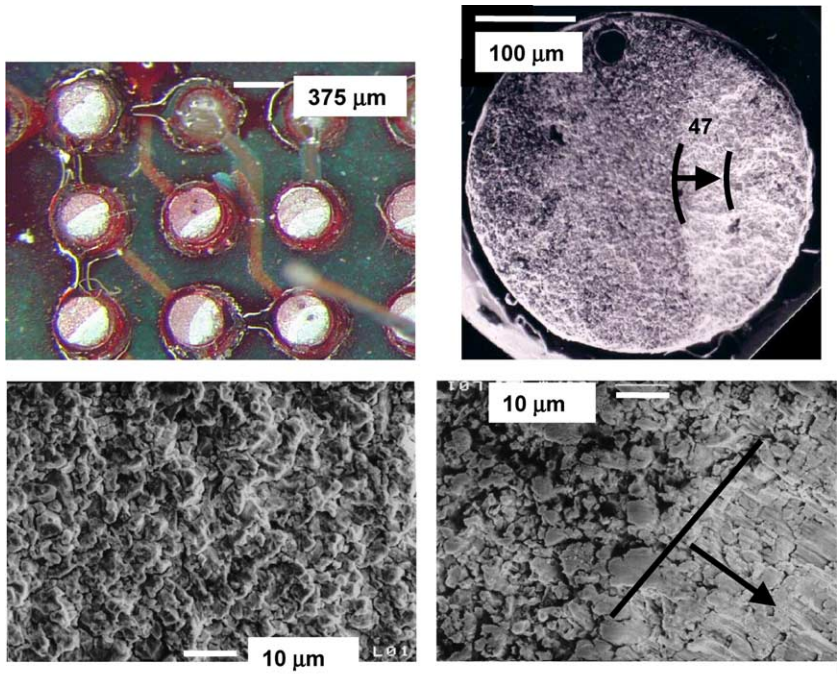

Fig. 6. Crack front observed at 2700th anisothermal cycle observed by injecting dye during the test. Top left image shows the varying extent of crack propagation among the different interconnects and the top right image shows the extent of separation in the critical solder interconnect. The bottom images are electron micrographs of the critical interconnection. The micrograph at bottom left shows the observed creep-fatigue microstructure and that on bottom right indicates the location at which the microstructure changed from that of creep fatigue to that corresponding to shear overload. The latter has characteristic streaks in the direction of the center of the component (neutral point).

substructure were interpolated from the displacements calculated on the appropriate planes of the global model (a full three-dimensional model of the entire package). The extracted boundary conditions were then assumed not to change during the crack propagation. In other words, the displacements imposed on any solder interconnection was assumed to be driven by a global thermal expansion mismatch between the assembled component and the circuit board, which were unchanged by the presence of a crack at the interface of the critical solder interconnection.

In the second set of models, an alternative analysis procedure was attempted. In the alternative procedure, the refined submodel of the critical solder interconnection was coupled to the rest of the assembly through multi-point constraints. This required considerably more computational effort since the reanalysis during crack propagation was not restricted to the critical solder interconnection alone.

At each iteration, two accelerated cycles were simulated to calculate the rate of disturbance change over the cycle. The accumulated disturbance value from the previous iteration (D_n in Eq. (9)) was then used to calculate the amount of disturbance that would be generated during the next $N_{n+1} - N_n$ cycles. The crack was predetermined to progress along the solder/metal pad interface. To take the disturbance accumulation in the material into consideration, the values of disturbance at one element row ahead of the current crack front were stored and added to the subsequent iterations until the critical disturbance value was reached, and then the nodal connectivity was released to create a new traction free surface.

Ideally, the crack is propagated by releasing the connectivity of one node (with critical damage value) at a time. However, it is prohibitively expensive to analyze a complete separation of bonded interface

consisting of a large number of interface nodes since the number of analyses required will be many times the number of interface nodes. Here, to achieve greater efficiency, rather than use a single critical disturbance value, a range of critical disturbance values was used. This allows multiple nodes to be released simultaneously at any iteration. If this range in critical disturbance value is made sufficiently small, the present procedure is expected to approach the ideal one with a single critical disturbance parameter value. In the present study, the simulations were carried out with two different fracture criteria to study the effect of critical disturbance range. The ranges 0.5–0.9 and 0.75–0.85 were chosen to release the connectivity of nodes in order to progress the crack. The accuracy of the chosen damage range was judged by the ability to predict crack trajectory during the fracture process and by the predicted fatigue life. To enable such a comparison, the crack front identified (by test) at the 2700th cycle (Fig. 6), through a dye that was injected into the crack, was used.

The fractured area in Fig. 6 was calculated by processing the image and was estimated to be roughly 70% of total interface area. Accordingly, the area of the crack faces in the finite element models was calculated to identify the predicted crack shape and associated fatigue life when the crack had progressed to 70% of the interface area. The analyses were continued until a complete separation of the interface occurred. The total number of cycles to failure was calculated by incrementally adding the number of cycles N_i required at each iteration to progress the crack.

4. Results and discussion

We begin by illustrating the strong correlation between the extent of crack observed experimentally and the maximum equivalent plastic strain in any solder interconnection in an intact assembly (Fig. 7). The area of crack was estimated based on images similar to that shown in Fig. 6. This is another justification for the use of Eq. (8) alternatively to Eq. (5) to predict crack initiation and progression.

The initial results were based on the analysis of a single solder interconnection using pre-determined boundary conditions obtained from a coarser three-dimensional analysis. When a critical disturbance range of 0.5–0.9 was used, the fatigue life at 70% cracked area was calculated to be 4460 cycles. Fig. 8 shows the distribution of inelastic creep strain dissipated along the predicted crack front of the critical solder interconnection (only half solder interconnection was modeled due to symmetry). A solid line is drawn connecting all the crack front nodes at the interface to indicate the predicted crack shape. The crack front shape is

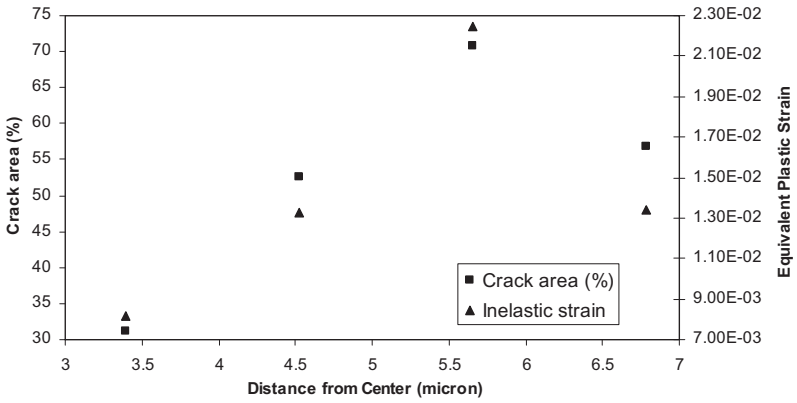

Fig. 7. Correlation between the observed crack area and the inelastic strain at solder interconnections located at various distances from the package center. The crack area was measured at 2700 cycles and the inelastic strain was calculated after the first cycle.

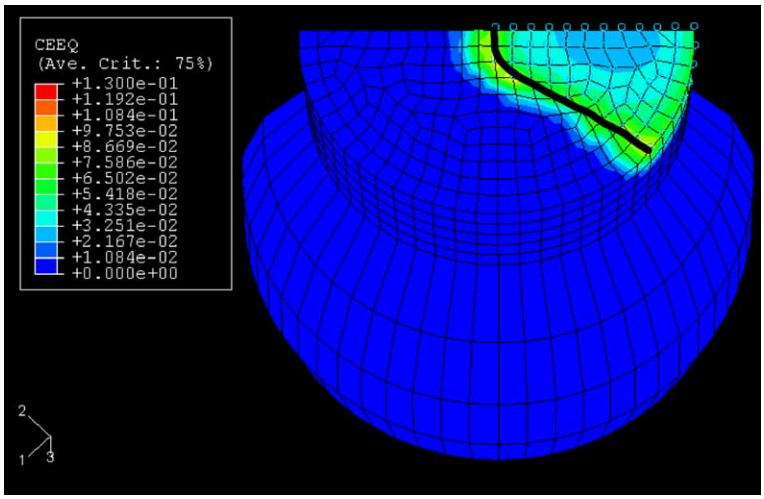

Fig. 8. The crack front predicted at 70% crack area through the use of a submodel and a critical damage range of 0.5–0.9.

clearly inaccurate compared to the actual front shown in Fig. 6. The crack appears to move faster in the circumferential direction in this simulation than in the experiment. Next, a narrower range in critical disturbance of 0.75–0.85 was applied. Although the predicted crack shape shown in Fig. 9 is more accurate than that in Fig. 8, the predicted life corresponding to the narrower critical damage range had a significantly larger error; the number of cycles corresponding to 70% cracked area was 5258 compared to the experimental value of 2700.

The possible sources for the error in the calculated fatigue life and the predicted crack shape as compared to the experimental results are: (1) insufficient mesh refinement (limited by the available computational resources) and (2) the approximation inherent in the submodeling technique that assumes that the re-distribution of stress and strain due to crack propagation does not affect the boundary conditions imposed on the interconnection.

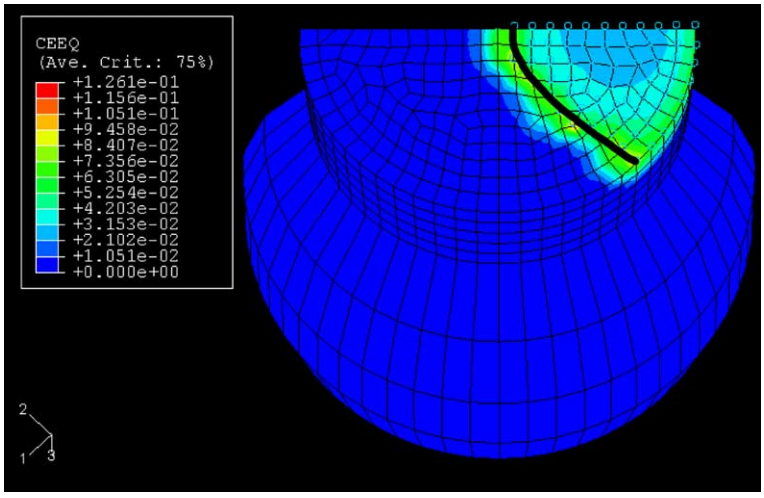

Fig. 9. The crack front predicted at 70% crack area through the use of a submodel and a critical damage range of 0.75–0.85.

To investigate the second possible source of error, a refined mesh corresponding to the solder interconnection was tied to the rest of the package using multi-point constraints (MPC). Even though this type of constraint significantly increases computational expense as compared to submodeling technique, it was unavoidable. The multi-point constraints allowed two dissimilar finite element meshes to be connected together by imposing displacement constraints on the surfaces. With a critical damage range of 0.5–0.9, the crack front in Fig. 10, from power cycling simulation at 70% cracked area is in good agreement with that in Fig. 6. The predicted crack trajectory is in excellent agreement with experiments when the damage range is smaller (Fig. 11). The two damage ranges did not result in significantly different predicted number of cycles for 70% crack area as can be seen from Table 1.

Similar to the anisothermal power cycling simulations discussed up to this point, the uniform temperature cycling test was also simulated using multi-points constraints. The submodeling technique was not applied to this case due to the inaccuracy observed earlier in power cycling simulations. Owing to the considerably longer dwell period at high temperature during the isothermal temperature cycling test, creep damage was larger and hence resulted in higher rates of disturbance change, $(\partial D/\partial N_n)$ in Eq. (9), and shorter fatigue life. The predicted fatigue life at complete separation was found to be 4,191 cycles.

One possible source of error in the predicted life is the values of the disturbance parameters ξ_c and z (Eq. (8)) used in this study. As mentioned earlier, these were average values over the range of −50 °C to +150 °C and were extracted from Sn–40 wt%Pb alloy test data while the modeled solder interconnections were made of eutectic Sn–37 wt%Pb alloy. In an attempt to estimate the impact of these material parameter values, the parameters were fitted so as to provide 2700 cycles corresponding to 70% cracked interface area. The new values for the parameters ξ_c and z were calculated to be 13.67 and 0.78, respectively. With the new disturbance parameters, the error in life prediction reduced from 30% to 3% for power cycling test but increased marginally from 11% to 12% for temperature cycling test. Decreasing values of ξ_c and increasing z imply a more rapid rise of damage with equivalent plastic strain in Eq. (8). This in turn implies that parameters corresponding to a higher temperature are more representative of the loading conditions than the average value between −50 °C and +150 °C that was used earlier in the simulations. In fact, the calculated ξ_c corresponds to the value of the parameter at a temperature of 77 °C, which is reasonable considering that the temperature excursion during the test was between 0 °C and 100 °C. The predicted isothermal and anisothermal test fatigue lives with the new values of the parameters are 3320 cycles and 3882 cycles, respectively.

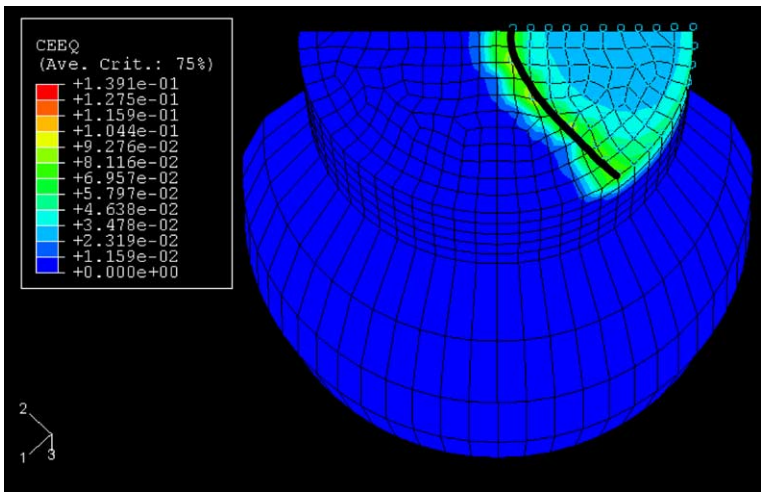

Fig. 10. The crack front predicted at 70% crack area through the use of multi-point constraints and a critical damage range of 0.5–0.9.

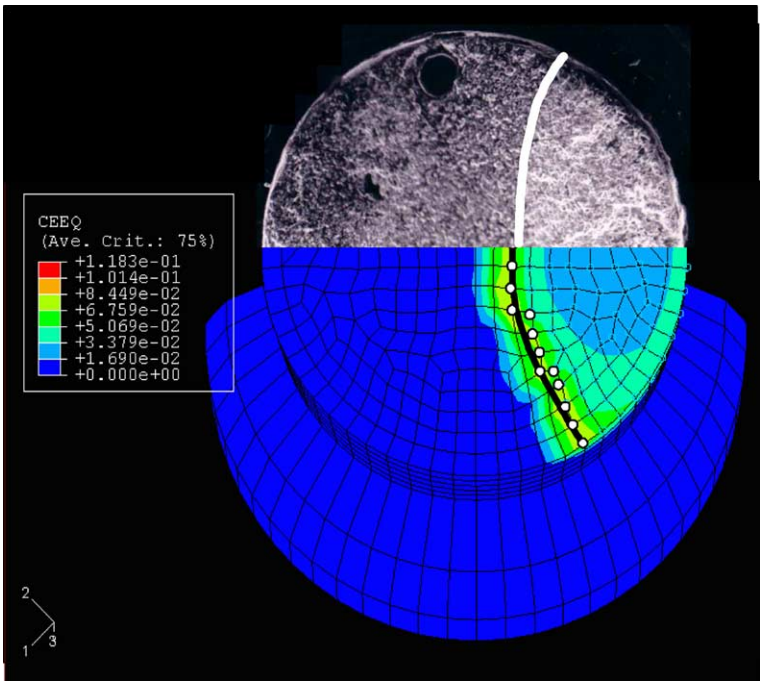

Fig. 11. The crack front predicted at 70% crack area through the use of multi-point constraints and a critical damage range of 0.75–0.85.

Table 1
Summary of fatigue life prediction

Predicted fatigue life	Anisothermal test					Isothermal test	
	FEA				Expt.	FEA	Expt.
	Submodel		Model with MPC			MPC	
	D: 0.5–0.9	D: 0.75–0.85	D: 0.5–0.9	D: 0.75–0.85		D: 0.75–0.85	
N_i at 70% cracked area	4460	5258	3416	3318	2700	N/A	N/A
% error	65	95	27	23		N/A	
N_f at L_{crit}	6557	6557	4532	4374	3770	3822	3570
% error	74	74	20	16		1	
Total no. of simulations	16	60	16	60		59	

Another important finding in the study is shown in Figs. 12 and 13. The plots illustrate disturbance change per cycle (damage rate) versus the normalized crack length along the centerline of the solder interconnection (Fig. 12) and along the circumference of the interconnection (Fig. 13). The disturbance rate in both directions were found to be nearly constant up to a point after which they were observed to rise at an exponentially higher rate, until the interface was fully separated.

Figs. 14 and 15 show a fit of the disturbance rate as a function of the normalized crack length for the anisothermal cycling test. When the crack reached a critical length, L_c, the disturbance rate increased exponentially. Most significantly, this computed critical crack length, L_c, agreed very well with the location at

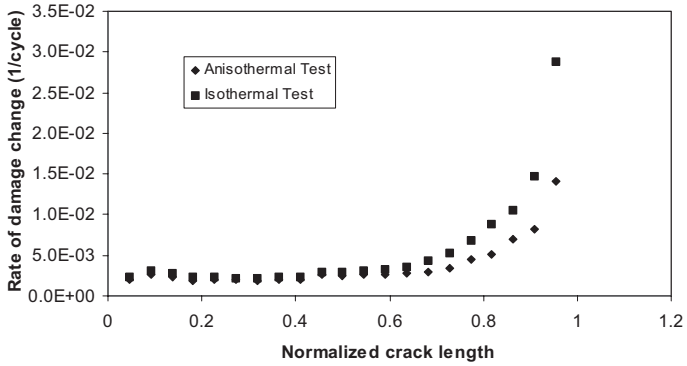

Fig. 12. The computed change in damage rate for a crack locus along the centerline of the solder interconnection.

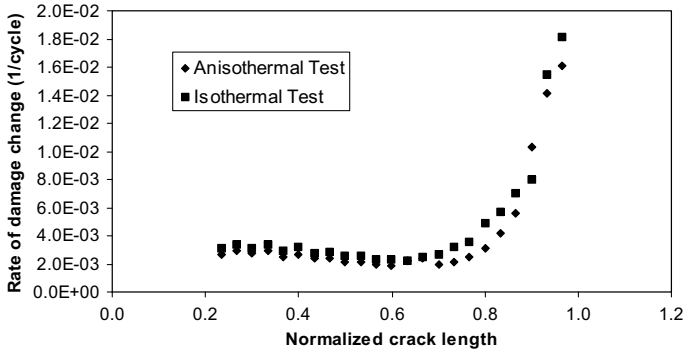

Fig. 13. The computed change in damage rate for a crack locus along the periphery of the solder interconnection.

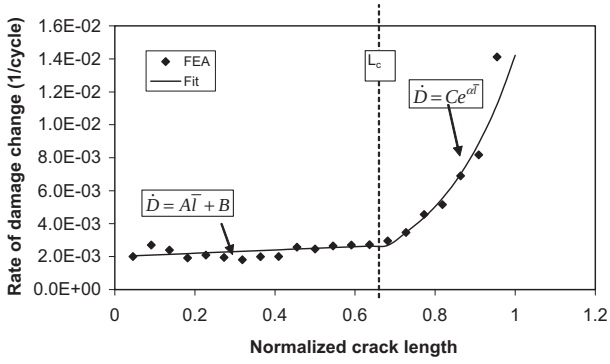

Fig. 14. Parameters describing damage change per cycle obtained through a fit to the data presented in Fig. 12.

which microstructural changes were observed on the failed interface (Towashiraporn et al., 2004a). At L_c, approximately 47 μm from the dye mark created during the 2700th cycle, the microstructure was observed to change from that due to creep fatigue to shear overload failure (see Fig. 6). The predictive power of the model is considerably enhanced by this ability to correlate with the microstructural changes. Such

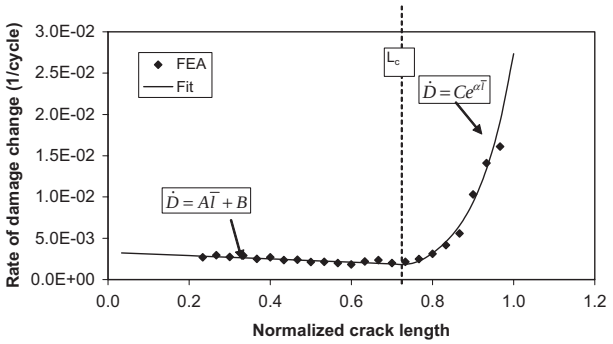

Fig. 15. Parameters describing damage change per cycle obtained through a fit to the data presented in Fig. 13.

Table 2
Summary of correlation constants in damage progression model

Locus	Parameters	Isothermal	Anisothermal
Centerline	A	2.00E − 03	1.00E − 03
	B	2.30E − 03	2.00E − 03
	C	1.00E − 03	8.00E − 05
	α	5.42E − 03	5.18E + 00
Periphery	A	−2.90E − 03	−2.00E − 03
	B	4.10E − 03	3.30E − 03
	C	3.30E − 05	6.00E − 07
	α	6.28E + 00	1.07E + 01

microstructural changes do not appear to have been captured in prior models. The crack growth mechanism deduced from the above models is the steady progression of a crack front whose shape is that of a circular arc until the critical crack length is reached. After the critical length was reached, the radius of the crack front decreases as the crack propagates since the damage rate is greater along the periphery than along the center (see Figs. 12–15). The calculated parameters A, B, C, and α from Figs. 14 and 15 are summarized in Table 2.

The results presented in Figs. 14 and 15 hint at the conditions under which an empirical, Coffin–Manson models such as that used by Darveaux et al. (1995), which relates the fatigue life N_f to inelastic dissipation ΔW in a cycle through a constant A as:

$$N_f = \frac{A}{\Delta W} \tag{10}$$

may be used to predict the fatigue life of a solder interconnection. The disturbance rate as can be seen from the figures is nearly constant up to the critical crack length. Furthermore, the exponentially increasing disturbance rate after L_c accounted for less than 10% of the total life. In other words, crack growth and consequent failure is rapid once the critical crack length is reached. This was true in both isothermal and anisothermal simulations.

5. Concluding remarks

A new computational procedure for fracture propagation based on the evolution of disturbance was proposed and used to simulate fatigue crack propagation in solder interconnections subjected to two different

environmental conditions. The accuracy of fatigue life estimation and the predicted crack trajectories show excellent promise in analyzing fatigue crack growth in bodies undergoing large plastic deformation. The damage progression in cohesive zone was found to evolve in a manner that is well characterized by the disturbance measure proposed earlier by Desai and co-workers. This damage definition was therefore used to make decision on crack progression along solder interface. The predicted crack shape showed excellent agreement with experimentally observed crack front. At least three conclusions may be drawn based on the results of the proposed approach. These are listed below:

1. Even though submodeling technique could save a substantial amount of computational effort in solving complex problems, it was found to be highly inaccurate in both fatigue life and crack front prediction when compared to a fully three-dimensional model using multi-point constraints. The approximation inherent in the submodeling technique—that the re-distribution of stress and strain due to crack propagation does not affect the displacement boundary conditions imposed on the interconnection was found to be invalid in the study.
2. A disturbance range of 0.5–0.9 can predict the fatigue life with the same level of accuracy as a disturbance range of 0.75–0.85 while substantially reducing the number of iterations necessary for crack propagation analysis. However, this disturbance range assumption of 0.5–0.9 cannot predict the crack fronts accurately. When the disturbance range is sufficiently small (i.e. 0.75–0.85), the solution approaches the one with single critical disturbance value while achieving greater efficiency.
3. The change in microstructure on the fractured surface of solder interconnection reported by Towashiraporn et al. (2004a) correlates extremely well with the exponential increase in rate of disturbance change per cycle calculated by the finite element analysis. Due to this rapid change in disturbance rate, the crack is expected to progress at a much faster rate after the critical length is reached. The rate of disturbance change was found to be nearly constant up to the point where microstructure change was observed. This implies that the crack growth rate is constant during most (90%) of the total number of cycles to failure. This in turn provides the basis for judging when empirical models may be applied with reasonable chance at success.

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